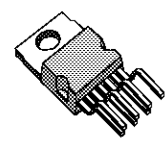
L4902A

DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS : I_{01} = 300 mA
  I_{02} = 300 mA
- FIXED PRECISION OUTPUT VOLTAGE 5 V ± 2 %
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1µA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION



HEPTAWATT (Vertical)

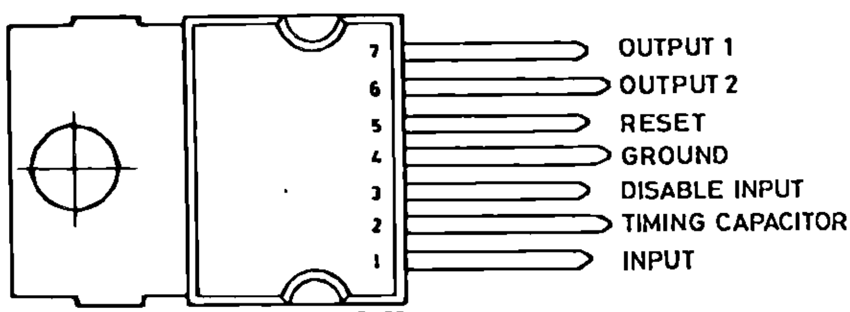
ORDERING NUMBER : L4902A

DESCRIPTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions and remote switch on/off control can be realized.

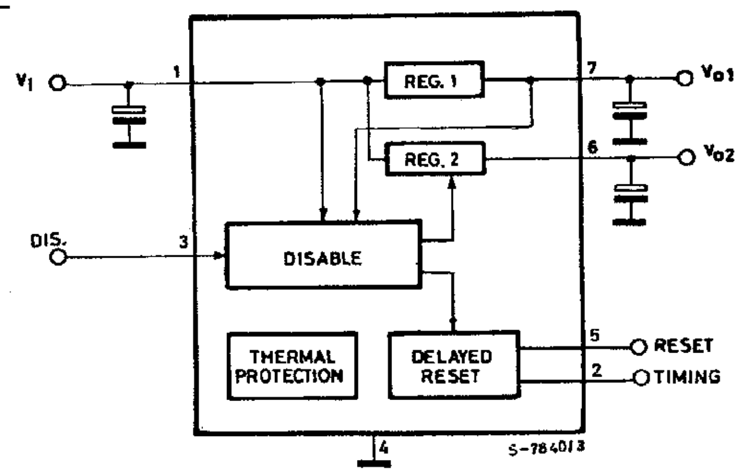
PIN CONNECTION



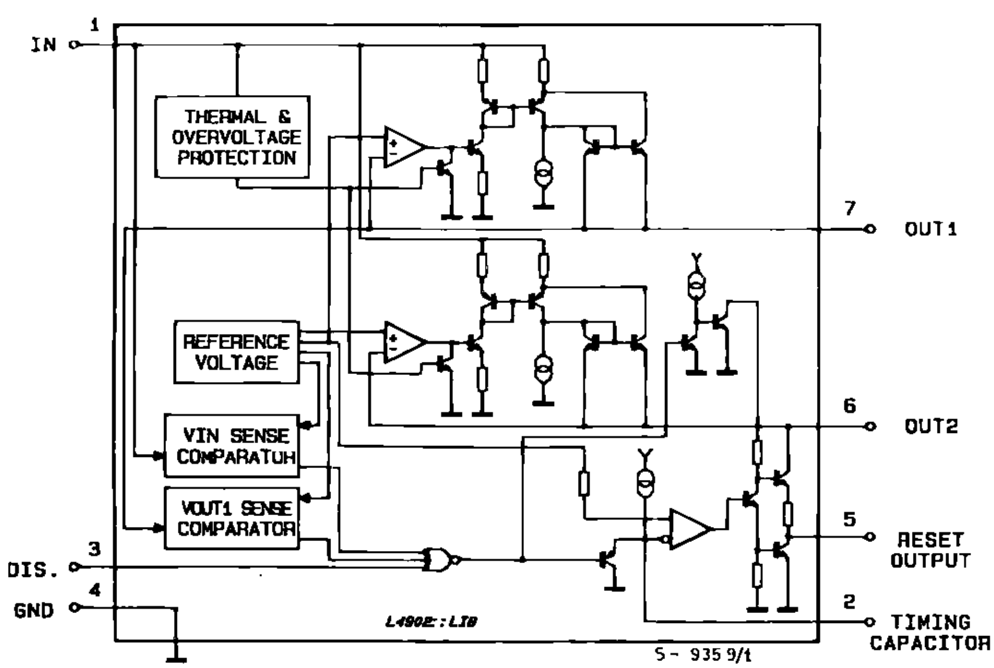
PIN FUNCTIONS

N°	Name	Function
1	Input 1	Regulators Common Input
2	Timing Capacitor	If Reg. 2 is switched-ON the delay capacitor is charged with a 5µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	Disable Input	A high level (> V_{DT}) disable output Reg. 2.
4	GND	Common Ground
5	Reset Output	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t\,(\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF)
6	Output 2	5V – 300mA Regulator Output. Enabled if V_o 1 > V_{RT}. DISABLE INPUT < V_{DT} and V_{IN} > V_{IT}. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	Output 1	5V – 300mA. Low leakage (in switch-OFF condition) output

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Transient Input Overvoltage (t = 40ms)	28 60	V V
I_o	Output Current	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

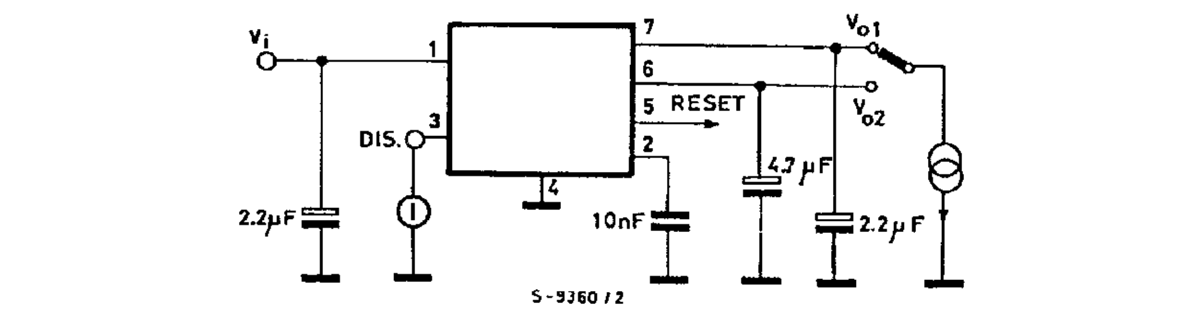
Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified))

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC Operating Input Voltage				24	V
V_{01}	Output Voltage 1	R Load 1kΩ	4.95	5.05	5.15	V
$V_{02\ H}$	Output Voltage 2 HIGH	R Load 1kΩ	V_{01} –0.1	5	V_{01}	V
$V_{02\ L}$	Output Voltage 2 LOW	I_{02} = – 5mA		0.1		V
I_{01}	Output Current 1 max.	ΔV_{01} = – 100mV	300			mA
I_{L01}	Leakage Output 1 Current	V_{IN} = 0, $V_{01} \le$ 3V			1	μA
I_{02}	Output Current 2 max.	ΔV_{02} = – 100mV	300			mA
V_{i01}	Output 1 Dropout Voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input Threshold Voltage		V_{01} + 1.2	6.4	V_{01} + 1.7	V
V_{iTH}	Input Threshold Voltage Hyst.			250		mV
ΔV_{01}	Line Regulation 1	7V < V_{IN} < 24V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line Regulation 2	7V < V_{IN} < 24V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load Regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load Regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent Current	$I_{01} = I_{02} \le$ 5mA 0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH		 4.5 2.7 1.6	 6.5 4.5 3.5	mA
V_{RT}	Reset Threshold Voltage		V_{02} – 0.15	4.9	V_{02} – 0.05	V
V_{RTH}	Reset Threshold Hysteresis		30	50	80	mV
V_{RH}	Reset Output Voltage HIGH	I_R = 500μA	V_{02} – 1	4.12	V_{02}	V
V_{RL}	Reset Output Voltage LOW	I_R = – 1mA		0.25	0.4	V
t_{RD}	Reset Pulse Delay	C_t = 10nF	3	5	11	ms
t_d	Timing Capacitor Discharge Time	C_t = 10nF			20	μs
V_{DT}	V_{02} Disable Threshold Voltage			1.25	2.4	V
I_D	V_{02} Disable Input Current	$V_D \le$ 0.4V $V_D \ge$ 2.4V		– 150 – 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 – 0.8		mV/°C
SVR1	Supply Voltage Rejection	f = 100Hz V_R = 0.5V Io = 100mA	50	84		dB
SVR2	Supply Voltage Rejection		50	80		dB
T_{JSD}	Thermal Shut Down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

TEST CIRCUIT



APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments ; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Figure 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs :

- a high level (V_{DT}) is applied on pin 3 ;
- an input overvoltage ;
- an overload on the output 1 (V_{01} V_{RT}) ;
- a switch off (V_{IN} V_{IT} - V_{ITH}) ;

and they start again as before when the condition is removed.

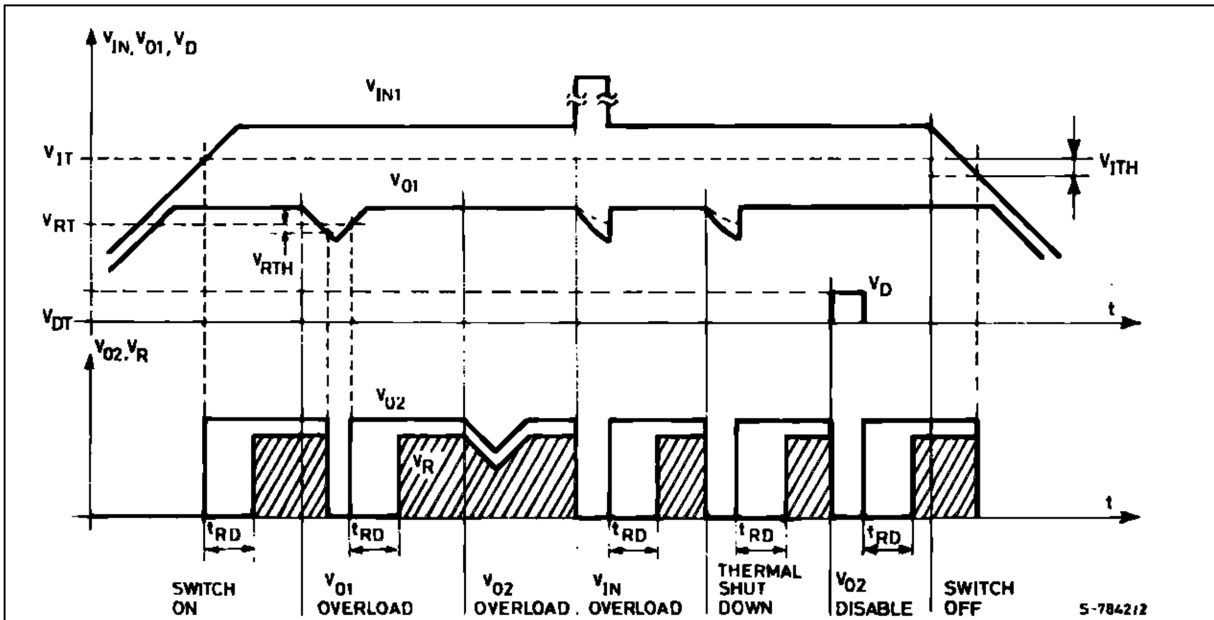
An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features :

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

Figure 1



This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

The V_{02} output can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

APPLICATION SUGGESTIONS

Figure 2 illustrate how the L4902A's disable input may be used in a CMOS µComputer application. The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS µcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a µP unit.

Figure 2

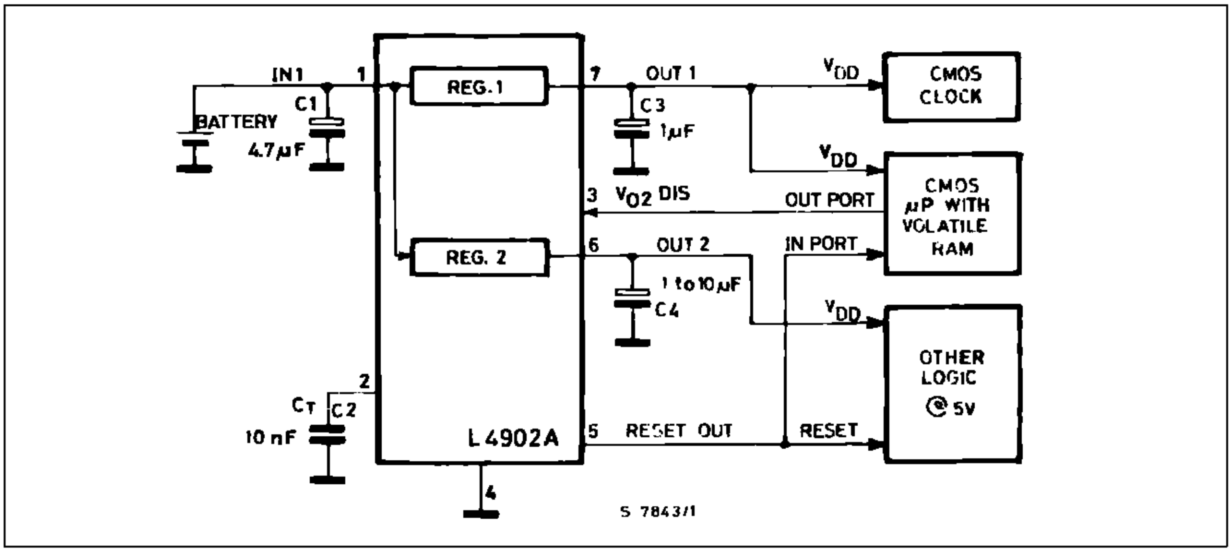
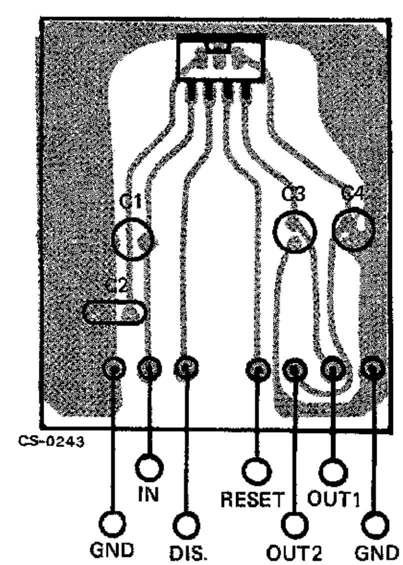


Figure 3 : P.C. Board Component Layout of Figure 2



Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for example) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see Figure 5). During normal operation the microsystem supplies a periodical pulse waveform ; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

Figure 4

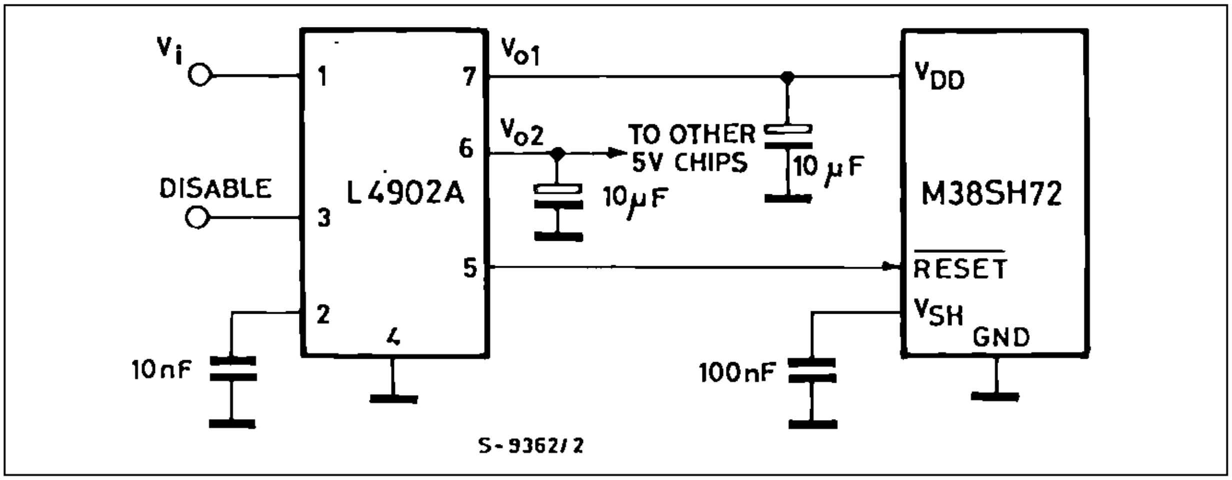


Figure 5

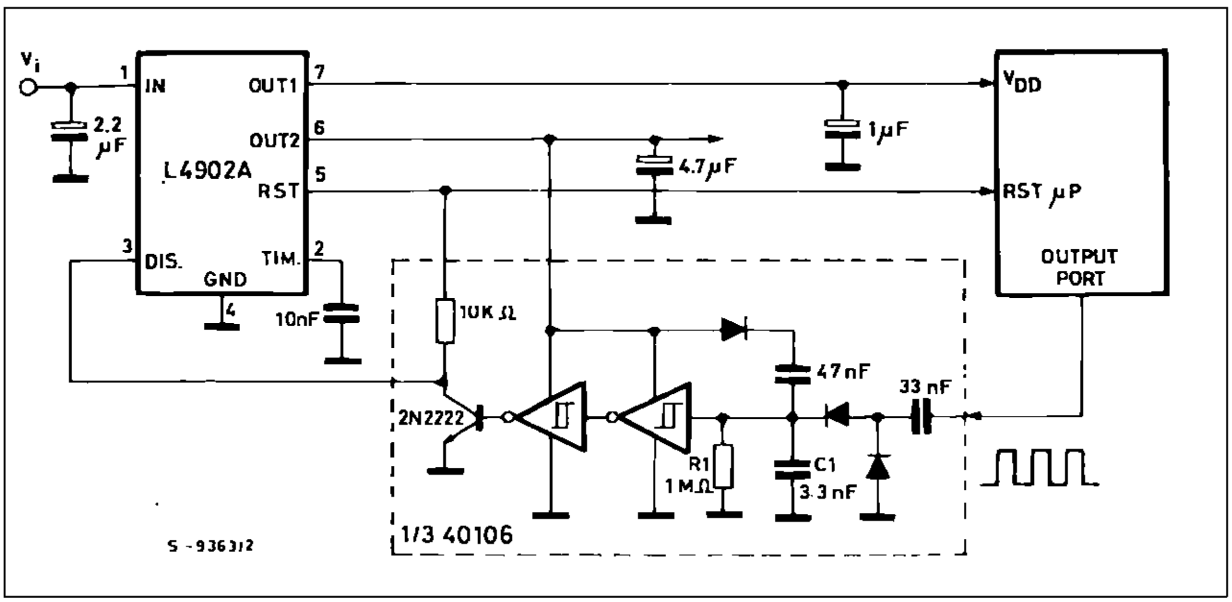


Figure 6 : Quiescent Current versus Output ICurrent

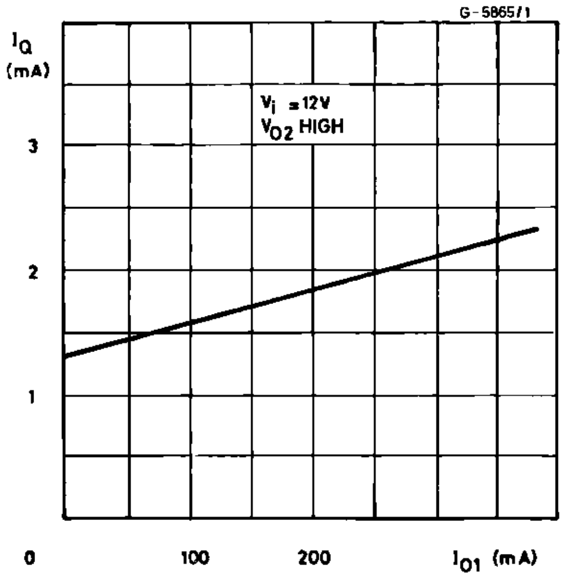


Figure 7 : Quiescent Current versus Input Voltage

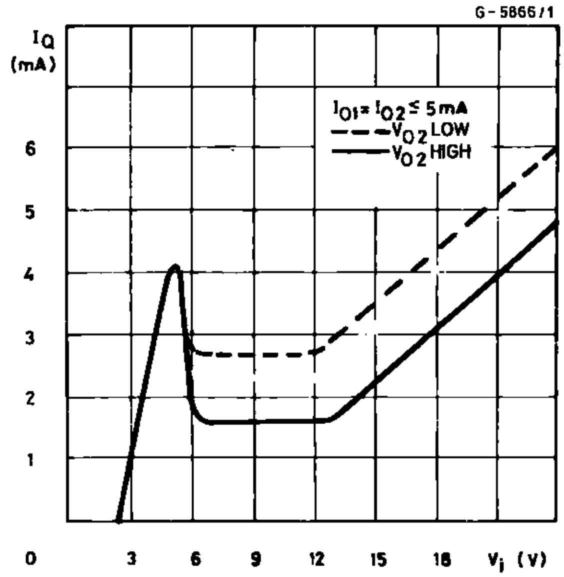
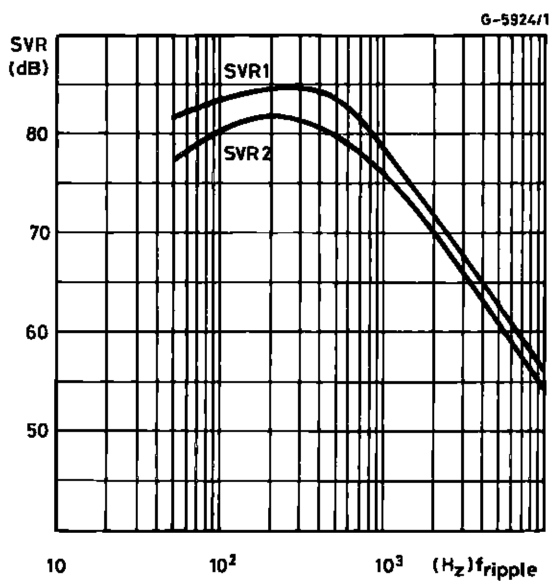


Figure 8 : Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequence



HEPTAVATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia	3.65		3.85	0.144		0.152

